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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,200	02/22/2002	Edward Allen Hall	RCA 89762	1634

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EXAMINER	
BHATTACHARYA, SAM	
ART UNIT	**PAPER NUMBER**
2687	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,200	HALL ET AL.	
	Examiner	Art Unit	
	Sam Bhattacharya	2687	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 8, 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 27, 28 and 30-35 are ~~is~~ are rejected under 35 U.S.C. 103(a) as being unpatentable over Badger (US 5,678,211) in view of Becker et al. (US 6,188,970).

As to claim 25, Figure 1 in Badger shows a tuner (10) comprising: first storage means (41) for storing alignment data for the tuner; and first control means including a phase-locked loop (28) coupled to the first storage means (see Col. 2, lines 4-54).

Badger fails to disclose that the phase-locked loop accesses the alignment data and the first control means utilizes the alignment data in performing tuner specific algorithms in response to a control signal from a second control means.

However, Becker et al. disclose tuning circuit that includes a memory 8' storing alignment data that is accessed by a phase-locked loop 7, which utilizes the alignment data in performing tuner specific algorithms in response to a control signal from a second control means 8. See FIG. 1, col. 2, lines 27-38, col. 5, lines 35-40 and col. 6, lines 32-40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to process the stored alignment data by the phase-locked loop circuit, as taught by Becker et al., in order to determine the shape of respective tuning curves and select an appropriate oscillator frequency for shaping the curves.

As to claim 27, Figure 1 in Badger shows the tuner of claim 25, wherein the first storage means is a first non-volatile memory. See col. 2, lines 4-54.

As to claim 28, Figure 1 in Badger shows the tuner of claim 25, wherein the nonvolatile memory is an EEPROM (see Col. 2, lines 48-54. The PROM 42 can be written via bus line 48 so it is functionally an EEPROM).

As to claim 30, Figure 1 in Badger shows the tuner of claim 25, further comprising a D/A converter (32, 34, 36) (see Col. 2, lines 27-30).

As to claim 31, Figure 1 in Badger shows the tuner of claim 25, wherein the tuner further comprises an address decoder (40) (see Col. 2, lines 27-30).

As to claim 32, Figure 1 in Badger shows the tuner of claim 31, wherein the address decoder includes a 1 to 1 actual channel to alignment channel addressing scheme (see Col. 2, lines 48-54).

As to claim 33, Figure 1 in Badger shows the tuner of claim 31, wherein the address decoder includes a plurality to 1 actual channel to alignment channel addressing scheme (see Col. 3, lines 44-59).

As to claim 34, Figure 1 in Badger shows the tuner of claim 31, wherein the address decoder is implemented using software (see Col. 4, lines 45-49. It is inherent that the processor means to retrieve data from the memory can be implemented in software).

As to claim 35, Figure 1 in Badger shows the tuner of claim 31, wherein the address decoder is implemented using hardware (see Col. 2, lines 27-30 and Figure 1).

4. Claims 26 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Badger in view of Becker et al. and Bonneau et al. (U.S. Patent 4,510,623).

As to claim 26, Badger-Becker shows the tuner of claim 25. However, it does not expressly disclose the phase locked loop circuit is a phase-locked loop integrated circuit. The Bonneau reference teaches the phase locked loop circuit is a phase-locked loop integrated circuit ("the description of the PLL 12 has been brief because such a device may be purchased as an off-the-shelf item, i.e., TD6306P, from Toshiba Corporation, and literature on the device is readily available" (Col. 4, lines 19-22)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the tuner of Badger-Becker wherein the phase locked loop circuit is a phase-locked loop integrated circuit, as taught by Bonneau, in order to use an off-the-shelf device for PLL.

As to claim 36, Badger-Becker discloses the tuner of claim 25. However, it does not expressly disclose the first control means is coupled to the second control means via an inter-integrated circuit bus. The Bonneau reference teaches the first control means (microprocessor) is coupled to the second control means (tuner module) via an inter-integrated circuit bus (see Col. 3, lines 18-24, Col. 4, lines 19-22, Col. 5, lines 2-4, and Figure 1. The PLL can be an IC and as part of a tuner, and the microprocessor can be another IC. Hence, the microprocessor is coupled to the tuner module via an inter-integrated circuit bus ("the microprocessor 13 supplies data and load commands to the PLL 12 via the PLL data bus 127" (Col. 4, lines 10-12)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Badger-Becker wherein the microprocessor is coupled to the tuner module via an inter-integrated circuit bus, as taught by Bonneau, in order to supply data and load commands to the PLL via the PLL data bus.

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Badger in view of Becker et al. and Bonneau et al., and further in view of Wu et al. (U.S. Patent 6,557,117).

As to claim 29, Badger-Becker-Bonneau discloses the tuner of claim 27. However, it does not disclose the re-writable memory is integrated in the phase locked loop integrated circuit. The Wu reference teaches the re-writable memory is integrated in the phase locked loop integrated circuit (see Col. 2, lines 55-65 and Figure 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Badger-Becker-Bonneau wherein the re-writable

memory is integrated in the phase locked loop integrated circuit, as taught by Wu, in order to test the PLL without external access.

Response to Arguments

6. Applicant's arguments filed on August 8, 2005 have been fully considered but they are not persuasive.

Applicant asserts that new claims 25-36 are allowable over the cited references. However, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Accordingly, Examiner maintains the rejection of new claims 25-36, for the reasons stated, over the same references previously applied in the rejection of canceled claims 1-24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Bhattacharya whose telephone number is (571) 272-7917. The examiner can normally be reached on Weekdays, 9-6, with first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester G. Kincaid can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sb

9/19/05

LESTER G. KINCAID
SUPERVISORY PRIMARY EXAMINER